WEST

End of Result Set

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L4: Entry 3 of 3 File: DWPI May 26, 1998

DERWENT-ACC-NO: 1998-321748
DERWENT-WEEK: 200158

TITLE: SRAM cell - includes resonant tunnel diode

INVENTOR: KARNIEWICZ, J; WU, J Z

PRIORITY-DATA: 1996US-0745458 (November 12, 1996)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5757051 A	May 26, 1998		023	H01L029/76

INT-CL (IPC): H01 L 29/76; H01 L 29/94; H01 L 31/062; H01 L 31/113

ABSTRACTED-PUB-NO: US 5757051A
BASIC-ABSTRACT:

The cell (500) comprises a p-type substrate (502) with a buried n-type layer (504). An n-channel transistor (506) with an n+ memory node (508), a gate (510) and an n+ digit line node (512) is formed over the layer with the memory node formed deeper in the substrate than the digit line node.

Two layers of alternating insulative (524,528) and conductive (526,530) material are formed near the source defining a resonant tunnel diode (522). Each insulative layer is a tunnel barrier. The upper conductive layer defines a terminal and the other conductive layer is a quantum well. The device is primarily in an ''off'' state. As voltage is increased, an ''on'' state is reached when a resonance condition is created. As voltage is further increased, another ''off'' condition is reached and then another ''on'' resonance condition.

ADVANTAGE - The SRAM is more compact and requires fewer MOSFETs than current SRAMs. The SRAM has more than two logic states which means an increase in bit density. It does not require refresh and has a smaller size.

WEST

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L5: Entry 1 of 1 File: DWPI Jan 3, 1997

DERWENT-ACC-NO: 1997-111513
DERWENT-WEEK: 199711

TITLE: Integrated circuit BiMOS fabrication method - uses monocrystalline silicon substrate covered by oxide layer and mask used to define n type buried regions generated by arsenic ion implantation

INVENTOR: COMBES, M; FOERSTNER, J ; HAUTEKIET, G ; MARTY, B A ; MARTY-BLAVIER, A

PRIORITY-DATA: 1995FR-0007904 (June 30, 1995)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
FR 2736208 A1	January 3, 1997		026	H01L021/8249
US 5691226 A	November 25, 1997		016	H01L021/8249

INT-CL (IPC): H01 L 21/8249

ABSTRACTED-PUB-NO: FR 2736208A
BASIC-ABSTRACT:

The method for manufacturing an IC consists in covering a monocrystalline silicon substrate (1) with an oxide layer and delimiting two buried n type regions. The two regions are defined by a masking operation. Arsenic ions are then implanted in the substrate areas revealed by an etching operation (20). An annealing treatment is then applied to the substrate.

A second masking operation covers the implanted areas which are associated with a NMOS component and a vertical PNP component. A high dose ion implantation is applied to the substrate in order to define N - and N+ regions.

USE - For manufacturing IC with CMOS and bipolar components on same substrate.

ADVANTAGE - Enables more complete integration of device manufacturing on same substrate.
ABSTRACTED-PUB-NO:

US 5691226A EQUIVALENT-ABSTRACTS:

The method for manufacturing an IC consists in covering a monocrystalline silicon substrate (1) with an oxide layer and delimiting two buried n type regions. The two regions are defined by a masking operation. Arsenic ions are then implanted in the substrate areas revealed by an etching operation (20). An annealing treatment is then applied to the substrate.

A second masking operation covers the implanted areas which are associated with a NMOS component and a vertical PNP component. A high dose ion implantation is applied to the substrate in order to define N - and N+ regions.

USE - For manufacturing IC with CMOS and bipolar components on same substrate.

ADVANTAGE - Enables more complete integration of device manufacturing on same substrate.

WEST

End of Result Set

Generate Collection Print

L6: Entry 1 of 1 File: DWPI Apr 22, 1997

DERWENT-ACC-NO: 1997-244463
DERWENT-WEEK: 199722

TITLE: Isolation structure for mixed mode semiconductor device - has continuous n=type regions with several p=type gaps, around p=type well with device built on p=type substrate

INVENTOR: JOARDAR, K; MONK, D J

PRIORITY-DATA: 1994US-0317078 (October 3, 1994), 1996US-0625685 (April 4, 1996)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5623159 A	April 22, 1997		007	H01L027/04

INT-CL (IPC): H01 L 27/04

ABSTRACTED-PUB-NO: US 5623159A
BASIC-ABSTRACT:

The isolation structure includes a p-type semiconductor substrate (12) with a p-type well (28) disposed in the substrate (12). Several continuous n-type regions (14, 16, 26) are disposed around the p-type well (28). The n-type regions (14, 16, 26) fully isolates the p-type well (28) from the substrate (12).

The continuous regions (14, 16, 26) comprise one or more p-type gaps (18) that electrically connect the p-type well (28) to the p-type substrate (12). Each gap has a minor dimension and the sum of the minor dimensions is less than about 3 microns.

ADVANTAGE - Improves cross-talk suppression in mixed-mode integrated circuits at higher frequencies, e.g. greater than 50 MHz, due to use of gap. It does not require internal contact for each well.

WEST

End of Result Set

Generate Collection Print

L3: Entry 1 of 1 File: DWPI Nov 2, 1999

DERWENT-ACC-NO: 1999-619665
DERWENT-WEEK: 200158

TITLE: Static memory cell manufacture

INVENTOR: KARNIEWICZ, J; WU, J Z

PRIORITY-DATA: 1996US-0745458 (November 12, 1996), 1997US-0948889 (October 10, 1997)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5976926 A	November 2, 1999		023	H01L029/76

INT-CL (IPC): H01 L 29/76

ABSTRACTED-PUB-NO: US 5976926A
BASIC-ABSTRACT:

NOVELTY - The memory cell includes a resonant tunnel diode.

DETAILED DESCRIPTION - The method comprises

(i) forming a buried n-type layer (504) having a first average n-type dopant concentration of at least 1x1016 ions/cm3, in a semiconductor substrate (502),

(ii) forming an n-channel transistor (506) relative to the substrate over the buried n-type layer, the transistor having a source, a gate, and a drain, the source having a second average n-type dopant concentration of at least 1x1019 ions /cm3 and the drain having a third average n-type concentration of at least 1x1019 ions/cm3, and the source having a depth greater than the drain so as to be closer to the buried n-type layer than the drain, and

(iii) forming layers (524, 526, 528, 530) relative to the source to define, in combination with the source, a tunnel diode (522).

USE - For static random access memory (SRAM) cell.

ADVANTAGE - The SRAM is more compact and requires fewer transistors. The memory cell has more than two logic states. By being able to store an increased number of logic states, bit-density can be increased. The SRAM does not require refreshing.

DESCRIPTION OF DRAWING(S) - The drawing shows a sectional view of a static memory cell.

Memory cell 500

Substrate 502

n-type buried layer 504

n-channel transistor 506

Memory node 508

WEST

End of Result Set

Generate Collection Print

L1: Entry 5 of 5 File: USPT Nov 2, 1999

US-PAT-NO: 5976926
DOCUMENT-IDENTIFIER: US 5976926 A

TITLE: Static memory cell and method of manufacturing a static memory cell

DATE-ISSUED: November 2, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wu; Jeff Zhiqiang	Meridian	ID		
Karniewicz; Joseph	Boise	ID		

US-CL-CURRENT: 438/237; 257/104, 257/314, 257/368

ABSTRACT:

A static memory cell having no more than three transistors. A static memory cell comprises a semiconductor substrate of a first conductivity type; a buried layer in the substrate, the buried layer having a second conductivity type opposite to the first conductivity type; a transistor formed over the buried layer, the transistor having a source of the second conductivity type, a gate, and a drain of the second conductivity type, the source having a depth in the substrate greater than the depth of the drain; and alternating layers of insulative and conductive material formed proximate the source, including two conductive layers and two insulative layers, one of the insulative layers being in junction relation to the source.

27 Claims, 20 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 13

WEST

End of Result Set

Generate Collection Print

L2: Entry 8 of 8 File: USPT May 26, 1998

US-PAT-NO: 5757051
DOCUMENT-IDENTIFIER: US 5757051 A

TITLE: Static memory cell and method of manufacturing a static memory cell

DATE-ISSUED: May 26, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wu; Jeff Zhiqiang	Meridian	ID		
Karniewicz; Joseph	Boise	ID		

US-CL-CURRENT: 257/368; 257/104, 257/25, 257/314

ABSTRACT:

A static memory cell having no more than three transistors. A static memory cell comprises a semiconductor substrate of a first conductivity type; a buried layer in the substrate, the buried layer having a second conductivity type opposite to the first conductivity type; a transistor formed over the buried layer, the transistor having a source of the second conductivity type, a gate, and a drain of the second conductivity type, the source having a depth in the substrate greater than the depth of the drain; and alternating layers of insulative and conductive material formed proximate -the source, including two conductive layers and two insulative layers, one of the insulative layers being in junction relation to the source.

34 Claims, 20 Drawing figures
Exemplary Claim Number: 34
Number of Drawing Sheets: 13